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J1036 U.S. PTO 09/932381 08/17/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: TI-31354

Serge Lasserre Art Unit:

Serial No: Examiner:

Filed: August 17, 2001

For: Local Memory With Indicator Bits to Support Concurrent DMA and CPU Access

INFORMATION DISCLOSURE STATEMENT

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Date of Deposit: August 17, 2001. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 CFR 1.10 on the date shown above and is addressed to: Ass't Commissioner for Patents, Washington, D.C. 20231.

Robin E. Barnum

Ass't Commissioner for Patents
Washington, DC 20231

Dear Sir:

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed PTO-1449. Copies of the noted references are enclosed herewith.

Since this IDS is being submitted before any Office Action, no fee is due.

Respectfully submitted,

Gerald E. Laws
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